Designing Video Circuits
Part Two

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Part One, which appeared in the October issue, described the fundamental concepts of video. This installment will discuss sampling standards—which standards are now available, and how to choose between them—as well as designs of synchronization and genlock circuits. Next month, the third and final segment will address the problems of producing video output from digital systems.

To ease video signal processing, it is useful to sample synchronously with the incoming video. The signal carries timing information in three portions of the waveform: horizontal sync, vertical sync, and subcarrier burst. H-sync relates harmonically to vertical frequency. This portion of the waveform provides timing information at every H-line, as does color burst; and so sampling is generally accomplished with clocking locked to either one or the other.

In subcarrier-locked sampling, the sampling pulse relates to color-burst reference phase and frequency. Sampling at three times subcarrier frequency (approximately 10.7 MHz for NTSC) fulfills the Nyquist constraint without excessive oversampling. A popular standard is to sample composite video at 8 bits at three times subcarrier frequency.

For NTSC, subcarrier (f_{sc}) and horizontal rates (f_H) are related by:

$$f_{sc} = 455f_H/2$$

In one horizontal line, there is an odd number of half-cycles of subcarrier. Alternately, this indicates that there is a 180° phase shift of subcarrier phase line-to-line.

If the sampling rate, f_s, is locked to burst and is three times the subcarrier frequency,

$$f_s = 3f_{sc} = 1365f_H/2$$

the sampling grid will advance 180° of the subcarrier per line. The grid will have a line-to-line offset of 46.7 nsec. At every other H-line, samples will line up one under the other (**Figure 1**).

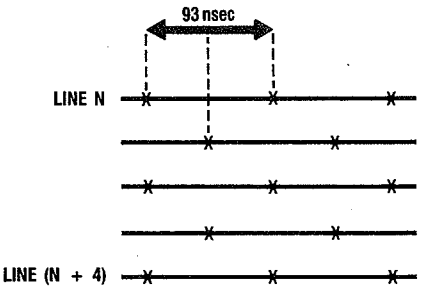


Figure 1: To ease processing of the video signal, the A/D converter can be used to sample synchronously with the incoming video. If the sampling rate f_s is locked to burst and is three times the subcarrier frequency, the sampling grid will advance 180° of the subcarrier per line. Every other H line, samples will line up one under the other.

Quite often, digital filtering is needed in the vertical dimension. If samples are not aligned vertically interpolation will be needed. This is a significant disadvantage of $3f_{sc}$ sampling.

With advances in A/D technology, four times subcarrier sampling (approximately 14.3 MHz) has become possible. Again, the subcarrier-to-H relationship can be written as:

$$f_s = 4f_{sc} = 4 \times 455f_H/2\, f_s = 910f_H$$

With this sampling rate, the sample pulse will have the same phase at the start of a horizontal line, and the sampling structure will be orthogonal in the horizontal and vertical directions.

Since each digital sample is associated with a defined value of subcarrier reference phase, it is relatively simple to decode the baseband color components from the modulated chrominance signal. For a chrominance signal sampled at $3f_{sc}$, multiplication of the digital waveform by subcarrier samples at 120° intervals will generate the baseband color signals. The original red, green, and blue camera signals can be recreated using simple addition and subtraction.

There are some drawbacks to subcarrier-locked sampling. A system that must deal with monochrome signals will not lock correctly, since there will be no color burst on which to reference the

sampling loop. Another problem is the processing of nonstandard composite systems. If there is no fixed relationship between subcarrier phase and horizontal sync, the sampling loop will alternately drift and lock. Also, for $3f_{sc}$ sampling, the sampling grid will not be orthogonal line-to-line, and digital interpolation may be needed for further processing. The use of $4f_{sc}$ produces a perfectly orthogonal sampling grid, but at the expense of a much higher sampling rate. For systems in which digital information is stored, the higher sampling rate requires 33% more memory space.

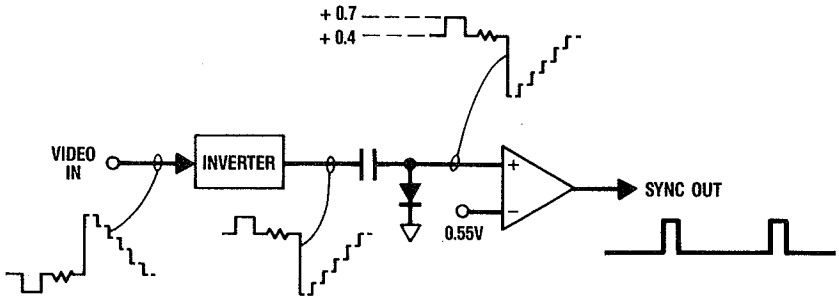


Figure 2: Implementation of a sync stripper. In operation, an inverter reverses the signal's polarity, causing the sync to be more positive than the active video. The capacitor and diode clamp the most positive excursion of the waveform to approximately 0.7V—the voltage of the forward-biased diode.

Component Versus Composite Standards

Roughly speaking, composite standards carry luminance and chrominance in a single shared-spectrum channel. Before display, the individual components of red, green, and blue must be decoded from the composite waveform. Composite systems have the advantage of a lower bandwidth and hence, in the digital domain, a lower bit rate. Three of the transmission standards in use worldwide (NTSC, PAL, and SECAM) are composite standards.

Composite video can be broken up into its individual parts using a decoder. Further processing takes place in the component realm. Component systems are generally three-channel systems; no modulation is used to carry luminance (Y) and color information. The component systems in common use today are RGB, YIQ, and Y, R-Y, B-Y. Because the baseband color signals can be generated without demodulation, complicated decoding processes can be avoided. Component processing is useful where high quality must be maintained from system to system. Before transmission, the three video components are encoded to form a more bandwidth-efficient composite signal.

Line-Locked Sampling

In line-locked sampling, the sampling clock is phase-locked to the horizontal synchronization pulse. A phase detector generates a control signal for a phase-locked loop (PLL) based on the phase difference between the sampling clock and a harmonic of H-sync frequency.

Parameters for component digital television signals have been standardized in CCIR Recommendation 601. The 4:2:2 standard is a system of coding for Y, R-Y, and B-Y digital components, where the sampling frequency is locked to a harmonic of the horizontal rate. Luminance is sampled at 13.5 MHz ($858 \times f_H$) and the color-difference signals are each sampled at half this rate.

Since the sampling clock is locked to horizontal sync edge, the phase of the sampling clock is ideally the same at the start of every line. Hence, samples are aligned vertically as well as horizontally. This perfectly orthogonal sampling grid eases digital filtering, since no interpolation is needed. The sampling rate is lower than the $4f_{sc}$ rate.

Another advantage of these systems is that the 13.5-MHz sampling rate for luminance is high enough for use in decoding both NTSC and PAL. There are the same number of active samples per line (720 for luminance, and 720 for chrominance) for both decoded PAL and NTSC. This makes it much easier to convert from one standard to another.

An important disadvantage of line-locked sampling is that there is no simple relationship between the sampling rate and reference subcarrier. For NTSC,

$$f_{sc} = 455f_H/2$$

If sampling is performed at $f_s = 858f_H$, then

$$f_{sc} = 455f_s/(2 \times 858)$$

This relationship is complicated compared to that of $3f_{sc}$ sampling, where the sampling pulse is related to only three positions on the subcarrier reference sinewave.

Synchronization

Synchronization pulses, or sync, occupy the bottom part of the composite video waveform. Horizontal and vertical sync are separated from the video signal by a sync stripper.

Figure 2 illustrates one implementation of a horizontal sync stripper. The video input signal is shown for negative sync polarity. The signal's dc level is indeterminate at this point, since prior processing may have occurred. An inverter reverses the signal's polarity, causing the sync to be more positive than the active video. The capacitor and diode clamp the most positive excursion of the waveform to approximately 0.7V (the voltage of a forward-biased diode).

The comparator is referenced to a dc voltage chosen to be the midpoint of the sync edge; this achieves best noise immunity. Sensing the swing of the sync edges, the comparator ignores the active video portion of the waveform. A train of pulses is then output with the same phase, width, and frequency of the sync pulse.

This function can be implemented digitally. If the sync edges are especially noisy, a technique that takes samples of the edges and averages them before threshold comparison will yield better noise immunity.

Genlock is the process of locking the timing of a video system

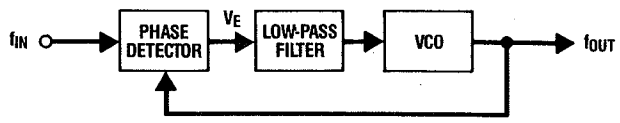
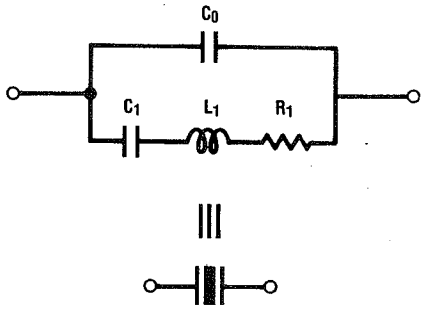
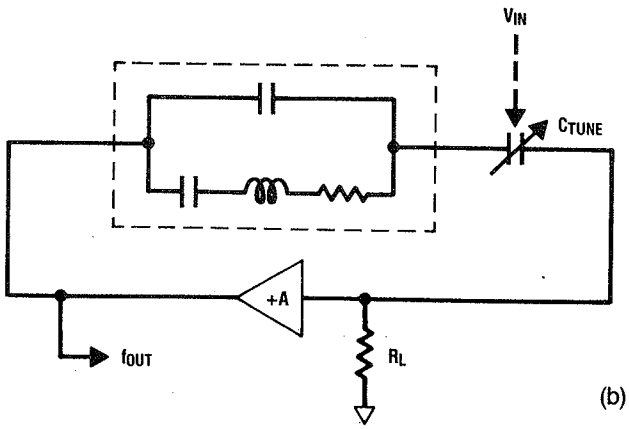


Figure 3: Phase-locked loops operate by first generating a voltage proportional to the difference between two periodic waveforms. This is accomplished by the phase detector. If the frequencies f_{IN} and f_{OUT} are not equal, the phase detector outputs a voltage that will force the VCO output frequency toward f_{IN}.



(a)



(b)

Figure 4: Quartz crystals are used as the basis of voltage-controlled oscillators. (a) These mechanisms can be modeled by a simple RLC circuit. (b) Equivalent representation of Figure 4a. In voltage-controlled oscillators, a reverse bias voltage on a tuning diode is used to dynamically vary the value of C_{TUNE}.

to an external reference. The sync stripper generates a pulse at a horizontal rate that is exactly in phase with the incoming reference. Timing references may be black-burst (a signal with the active video at black level) or a standard video signal.

The genlock process also works for vertical sync and/or color burst. Color burst is used for digital video systems that employ subcarrier-locked sampling. Alternatively, a line-locked sampling structure can be used, in which the sampling clock is locked to horizontal sync using a phase-locked loop synthesizer.

Phase-Locked Loops

Phase-locked loops are essential elements of most video systems (**Figure 3**). PLLs are different from other control systems. One element of the PLL is the voltage-controlled oscillator (VCO), which provides an output frequency proportional to input voltage. In operation, a phase detector generates a voltage proportional to the phase difference between two periodic waveforms. If the frequencies f_{OUT} and f_{IN} are not equal, the phase detector will output the voltage, and it will force the VCO output frequency toward f_{IN}.

Voltage V_e contains noise and harmonics of the input frequency. This is filtered, and a dc signal is applied to the VCO. The VCO output is a frequency proportional to the input voltage. When the loop is locked, the output frequency equals the average frequency of the input signal. PLLs reject noise on the input signal, and produce a cleaned-up version of the input frequency.

The VCO requires a frequency-selective element to tune its center frequency to the correct value. A quartz crystal can be used as the tuning element. Quartz exhibits the piezoelectric effect; that is, motion of the crystal matrix produces a voltage, and vice

versa. Motional waves in the crystal can be driven by an applied electric field, and in turn produce a voltage. The mechanisms of the quartz matrix can be modeled by a simple RLC circuit (**Figure 4a**). R_1, L_1, and C_1 are motional parameters associated with the mechanical characteristics of the crystal matrix and the particular crystal cut. At series resonance, the series reactance of the crystal is at a minimum (R_1). C_0 is the static capacitance of the crystal leads, and of the metal contacts bonded to the crystal surface.

Figure 4b shows an equivalent representation of a voltage-controlled crystal oscillator (VCXO). At series resonance, the impedance of the crystal is at a minimum, and the loop gain is positive and sufficiently large to sustain oscillation. The series resonant frequency can be varied slightly by changing C_{TUNE}. In a VCO, a reverse-bias voltage on a tuning diode is used to dynamically vary the value of C_{TUNE}.

As an inexpensive, stable source of frequency, crystal oscillators are unsurpassed. LC oscillators can be designed with stabilities of 0.01% or so; the high Q of a crystal enables frequency stabilities of a few parts per million. This high degree of precision is often needed for video processing, as only a few nanoseconds of phase shift can be visible to the viewer. For this reason, all video test signal generators rely on crystal-controlled oscillators to regulate their time bases.

Line-Locked Clocks

For NTSC, the CCIR 601 standard provides for a sampling rate, f_s, that is the 858th harmonic of the horizontal rate. That is, $f_s = 858f_H = 13.5$ MHz. The horizontal rate for NTSC is 15.734 kHz. A PLL can be used to synthesize the sampling clock at 13.5 MHz

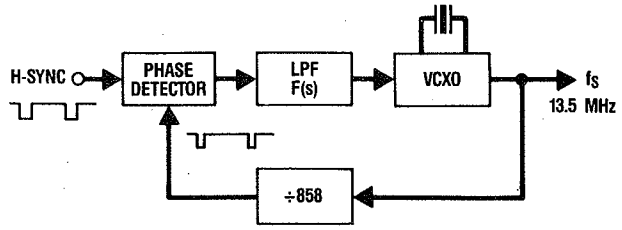


Figure 5: Line-locked frequency synthesis. In NTSC, CCIR 601 specifies a sampling rate that is the 858th harmonic of the horizontal rate. By using a PLL, the sampling clock of 13.5 MHz can be synthesized.

(**Figure 5**). The input to the system is the stripped horizontal sync pulse train from the sync stripper. The filtered voltage from the phase detector is fed to a VCO with a center frequency of 13.5 MHz. The output of the VCO is fed to the A/D converter to clock the video sampling.

Clock rate f_s is divided down by a factor of 858 by digital methods. Divider output, which is at approximately horizontal rate, is compared with the input frequency. The phase detector produces a voltage proportional to the phase difference, and negative feedback forces the phase error toward zero. Closed-loop dynamics and noise performance are determined primarily by the filter transfer function F(s). **ESD:**

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